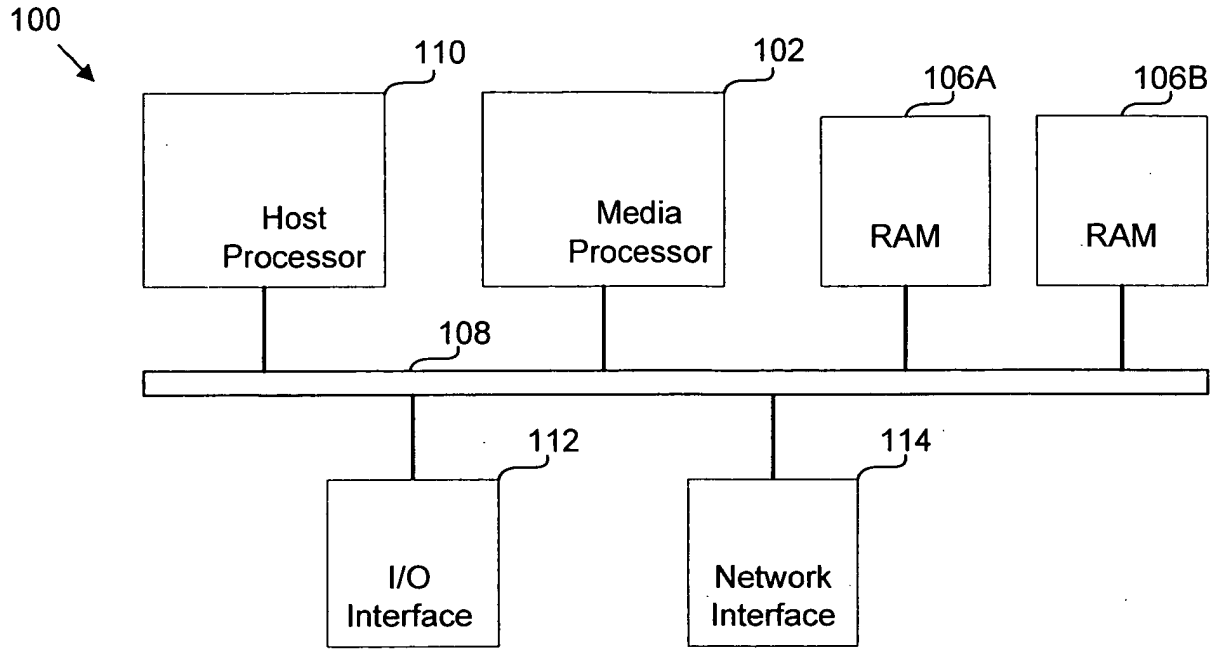

Figure 1

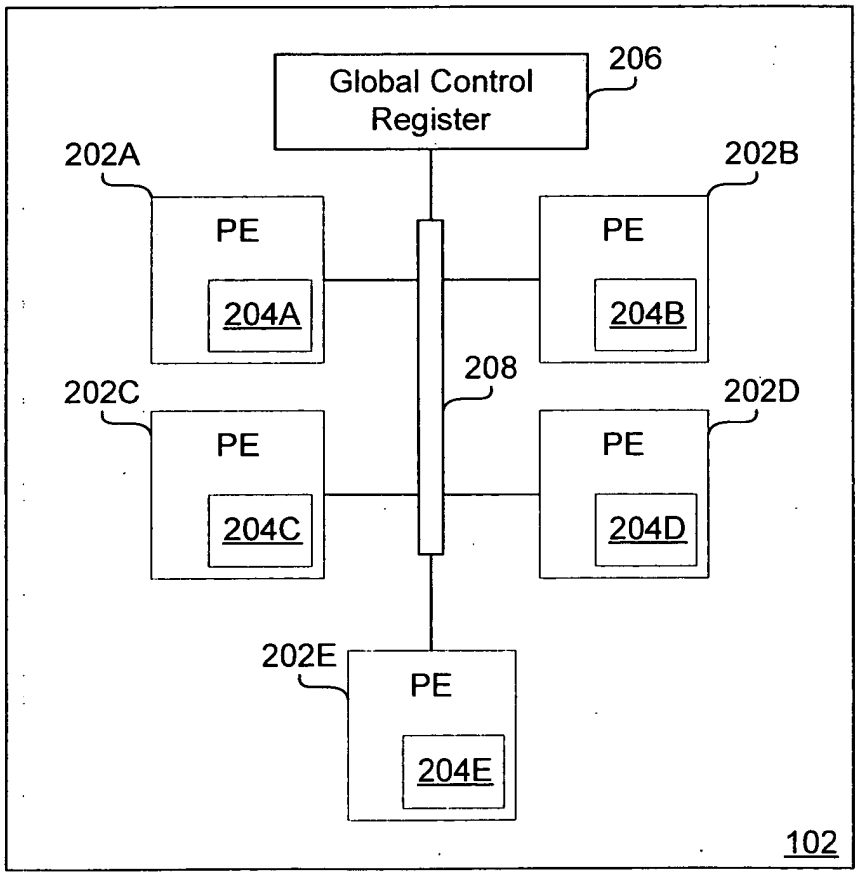

Figure 2

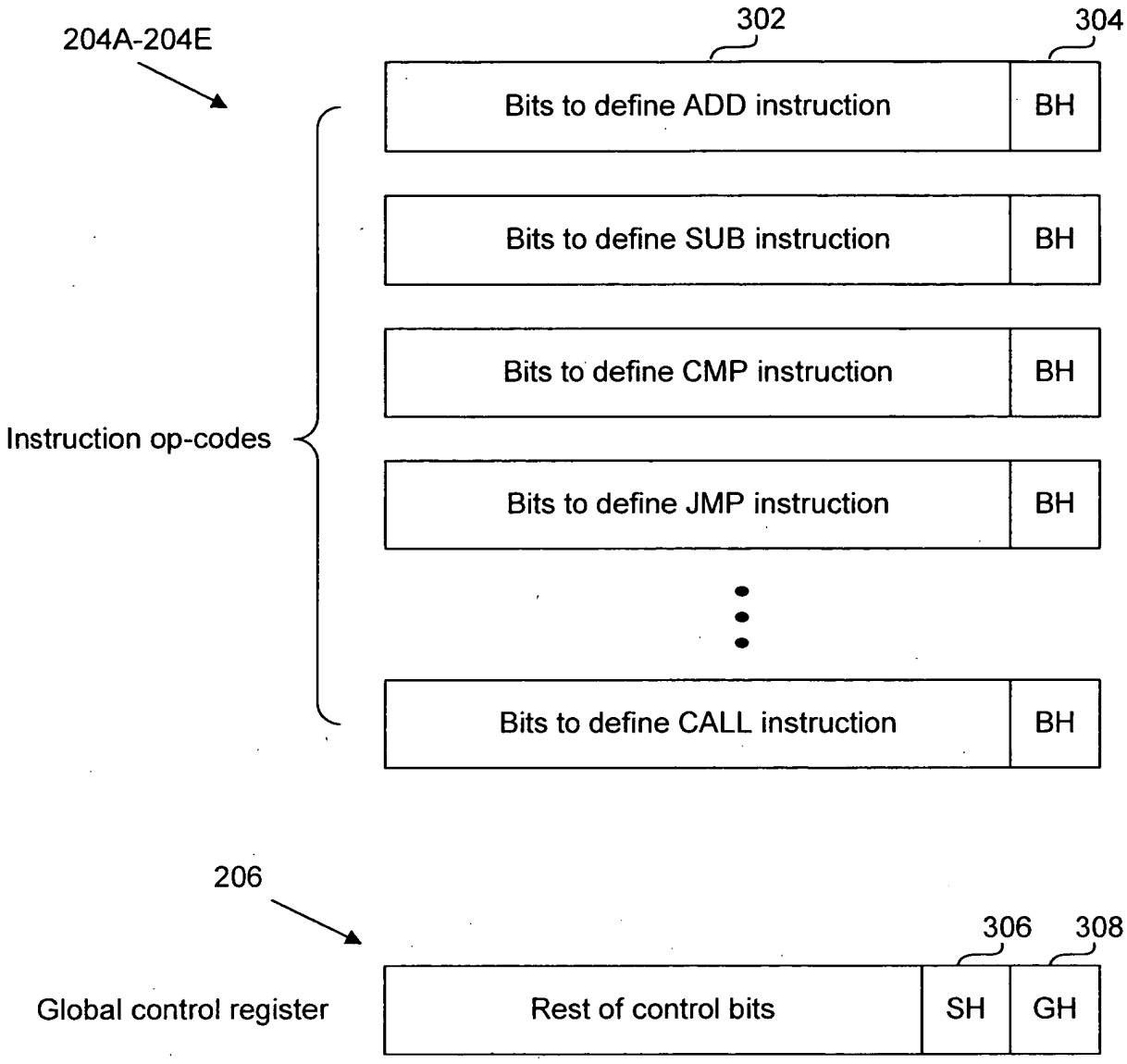
204A-204E
302
304
Bits to define ADD instruction
BH
Bits to define SUB instruction
BH
Bits to define CMP instruction
BH
Instruction op-codes
Bits to define JMP instruction
BH
Bits to define CALL instruction
BH
206
306
308
Global control register
Rest of control bits
SH
GH

Figure 3

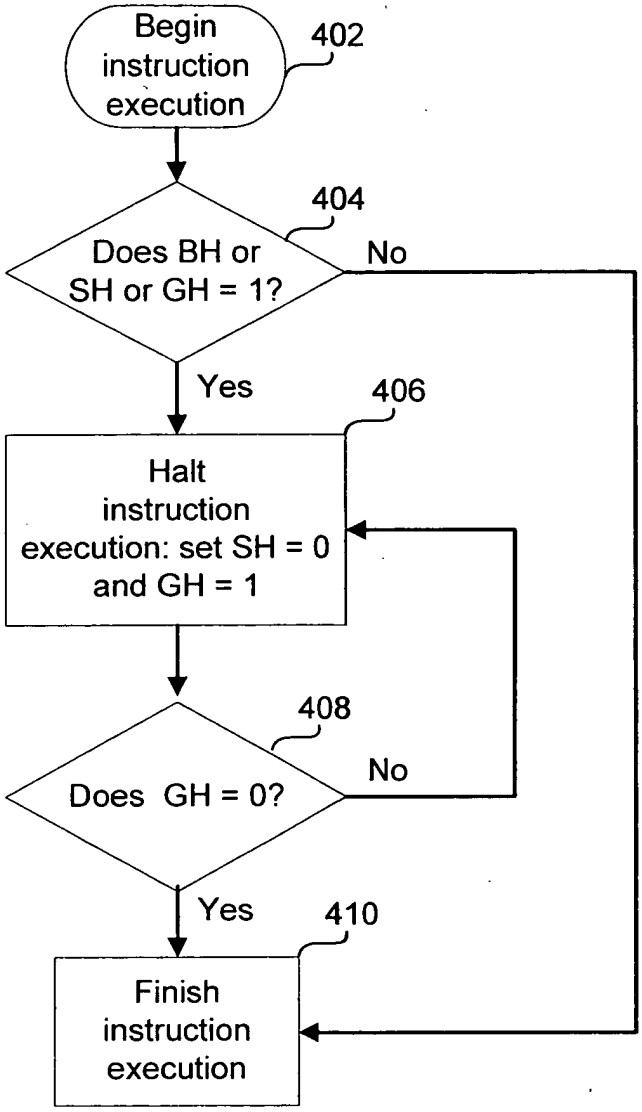
Begin instruction execution
402
Does BH or SH or GH = 1?
404
No
Yes
406
Halt instruction execution: set SH = 0 and GH = 1
Does GH = 0?
408
No
Yes
410
Finish instruction execution

Figure 4

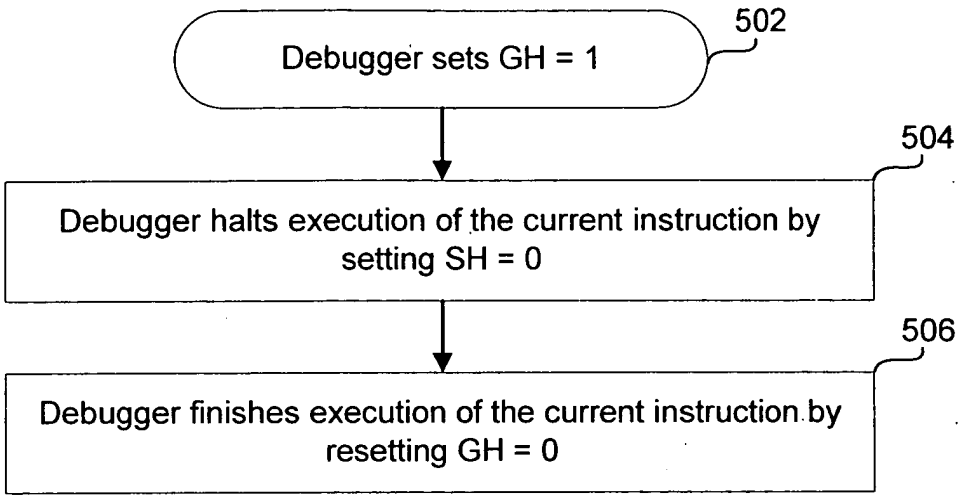

Figure 5

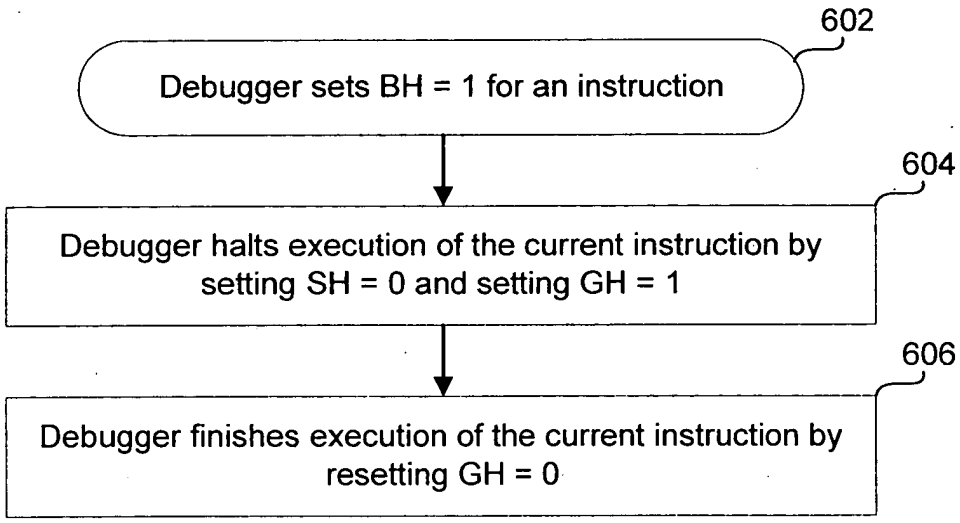

Figure 6

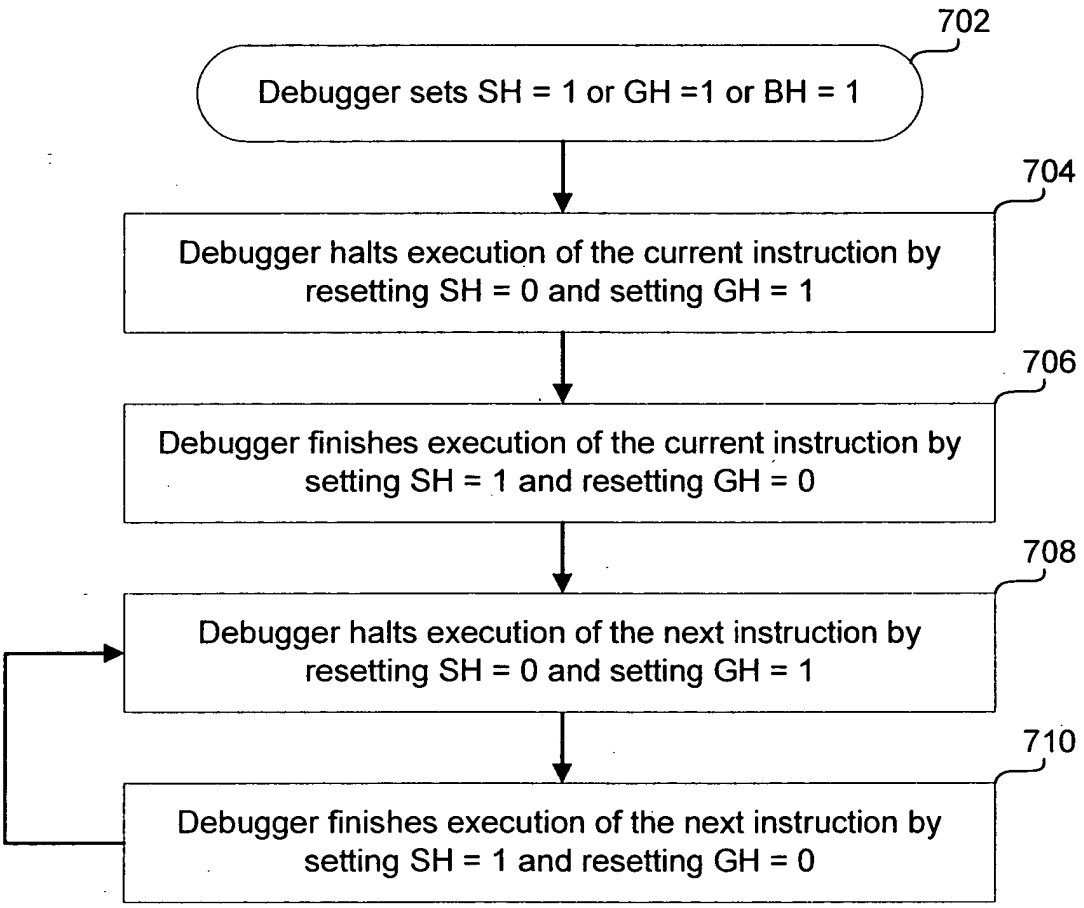
702
Debugger sets SH = 1 or GH =1 or BH = 1
704
Debugger halts execution of the current instruction by resetting SH = 0 and setting GH = 1
706
Debugger finishes execution of the current instruction by setting SH = 1 and resetting GH = 0
708
Debugger halts execution of the next instruction by resetting SH = 0 and setting GH = 1
710
Debugger finishes execution of the next instruction by setting SH = 1 and resetting GH = 0

Figure 7